Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

DESIGN OF POWER EFFICIENT 10 BIT 150MS/s SAR ADC IN 90NM CMOS TECHNOLOGY

MANJUNATH PATIL,
Ramaiah Institute of Technology, Department of Electronics and Communication Engineering, Bengaluru, India.
manjunathpatil16@gmail.com

M. NAGABUSHANAM,
Ramaiah Institute of Technology, Department of Electronics and Communication Engineering, Bengaluru, India.
nagabushanam1971@msrit.edu

M. C. PARAMESHWARA,
Vemana Institute of Technology, Department of Electronics and Communication Engineering, Bengaluru, India.
pmcvit@gmail.com

ABSTRACT: As the use of digital systems grows, so does the demand for converting analog data to digital data. Because of its moderate conversion speeds, good resolution, and small die area, Successive Approximation Register (SAR) Analog to Digital Converters (ADC) are commonly used. Data converters are essential for converting analog signals to digital signals. Due to its good balance of power, area, and speed considerations, SAR ADC is the most recommended architecture for ADC implementation. A unique high gain operational amplifier is presented as a comparator for a 10-bit SAR-ADC in the presented work. This work implements the 10-bit SAR-ADC with a D flip-flop (Delay flip-flop) based SAR logic, a high gain operational amplifier as a comparator, and a Report to Report (R2R) Digital to Analog data-converter (DAC). The work is implemented in Cadence Exploratory Data Analysis (EDA) utilizing the gpdk090 library in 90 nm CMOS (Complementary Metal-Oxide-Semiconductor) technology. The Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) are determined to be less than 1LSB (Least Significant Bit) on average. With a sample rate of 150 MS/s and a supply voltage of 1 V, the ADC consumes 265.8 µW of power with Effective Number of Bits (ENOB) of 9.39 bits and Signal Difference to Noise Ratio (SNDR) of 58.2dB. The SAR ADC that has been presented uses less power and can be used in portable devices.

Keywords: Digital to analog converter (DAC), Successive approximation register (SAR), SAR logic, Sample and hold circuit, comparator.

1 INTRODUCTION

In the present, day–to-day hectic life, in numerous, as well as a wide variety of electronic equipment are extensively. used in various fields of work that includes every field of activity from use of domestic appliances to space travel, imparting basic education to conducting complex research, wrist watches providing health parameters to sophisticated state-of the art medical equipment [1] and the like. Evidently, its deployment is not just limited to use in entertainment, transportation,

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

navigation communication etc. Today, every single step can be viewed, monitored and recorded by electronic equipment located across the globe. That is the role that electronics plays in our lives today. The vital and important components in these electronic equipment are the data converters that are mainly digital-to-analog converter and analog-to-digital converters. As all are very much aware, that most of the signals in real world are analog and the two data converter blocks; Digital-to-Analog Converter' (DAC) and `Analog-to-Digital Converter' ADC [2] play a crucial role by facilitating electronic equipment to process the procured analog signals and convert them to equivalent digital signals that can be easily understood and processed by most of the digital electronic equipment. ADCs are the vital elements in the design of power in electronic devices. Particularly in the field of 'Implantable' medical electronic devices such as cardiac defibrillators and pacemakers, ultra-low power consumption [3] is not just an important but a vital factor. On the one hand research and technological developments have provided better, long lasting batteries which if are augmented by low consumption devices, the implants could be made to last much longer providing relief to patients. If an implant lasts a lifetime, the patients would welcome it. The ADC in biomedical application can be designed using various architectures but what makes designers prefer 'Successive-Approximation-Register' (SAR) architecture over other architectures are its parameters, such as low sampling frequency and good functioning even with moderate resolution, that it offers. Another important noteworthy aspect is that the SAR architecture consumes much less power on account of its quite simple structure. SAR-ADC is made uniquely adjustable with the scaling technology facilitated by the blocks in the SAR-DAC which mostly are digital, except for the comparator.

2 LITERATURE SURVEY

Great efforts are made to develop Very Large-Scale Integration (VLSI) systems like DAC's and ADC's that have been one of the most volatile and dominant ones even today in terms of high-power efficiency, resolution and speed. This section provides an insight into the research works developed in the last few years to achieve better converter design. Zhang Hao et al. [4] have proposed and implemented 120 MS/s, 10-bit, single channel SAR ADC in 90nm 'complementary metal oxide semiconductor' (CMOS) technology. They have made use of partial monotonic switching sequences by which they were able to achieve significant reduction in common mode voltage variation. To overcome the problem of comparator errors which are caused due to DAC settling and dynamic offset, authors have deployed binary redundancy compensation technique. The author claims that in comparison to conventional structure the method proposed by authors enhances speed, decrease chip area and on top of all these, it reduces capacitance by 4 times. As per the simulation data given in paper, the author was able to achieve 'effective number of bits' (ENOB) of 9.72 Bits at a sampling rate of 120 MHz with input signal frequency 58.134 MHz, SNDR of 60.27dB, with power consumption of 3.24mW. Liu Haizhu and Maliang Liu [5] proposed a pipelined SAR hybrid ADC architecture with a 12-

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

Bits resolution and sampling rate of 200 MS/s.A 3.5-bit Multiplying Digital to Analog Converter (M-DAC) is used as first stage, and there is a 9-Bit SAR ADC as second stage. The author proposes using a Class-AB residual amplifier of high DC gain, in the MDAC stage to obtain a DC gain of 80 dB and a Unity Gain Band width of 0.8 GHz. This architecture, according to the author, has a 0.21mm2 footprint and consumes 7.3mW of power. At 200 MS/s, the author obtained 71.2dB 'Spurious Free Dynamic Range' (SFDR) and 61.9dB Signal-to-noise distortion-ratio(SNDR). Singh et al. [6] have proposed a power efficient, high speed SAR-ADC designed using 90nm process node. To achieve increase in device speed and for significant reduction in power consumption, authors have made use of a dynamic Double tail latched type comparator instead of using a conventional comparator. As per the simulation results given in paper author was able to achieve 0.98mW power consumption for his proposed architecture. Hequan Jiang et al. [7] have proposed a linearity enhanced 160MS/s, SAR ADC of 10-bit resolution that has low-noise and high-speed comparator. In order to enhance sampling switch linearity, the technique of floating p-well is exploited. As a result, there is overall reduction in parasitic capacitance of sampling switch. In order to achieve comparator noise reduction at higher rates of conversion a technique "Voltage boosting of substrate" is exploited. The author has presented an adaptive sampling approach to enhance the sample time of SAR-ADC. According to results of simulation included in the paper, the author was able to obtain a power consumption of 2mW, an SNDR of 55.6 dB, and an SFDR of 69 dB at 160MS/s. The core of ADC has 0.023mm^2 of active area. Xie Yi, et al. [8] have presented hybrid architecture combining SAR and Voltage Controlled Oscillator (VCO). The authors have made use of body effect compensation technique to improve the reliability and linearity of the bootstrapped switch. To optimize the DAC settling time, variable time control cell with asynchronous clock generation circuit is presented. This method has achieved SNDR of 56.7 dB, SFDR of 72.2 dB for 5 MS/s sampling rate.

The main goal of the proposed paper is to improve sampling rate higher than 100 MS/s compared to the literature and to achieve further improvement in the SNR, ENOB. As shown in table 1, In the base paper [9] the SAR-ADC is implemented in 90nm CMOS process technology with sampling rate of 120 MS/s, 10-bit resolution and have power consumption of 3.24mW, SNDR of 60.27dB and ENOB of 9.72-bits. The only attractive choice for medium resolution and low power is the SARADC converters; these approaches provide better power efficiencies. The literature summary in table 1 shows that the proposed converters use conventional type of switching schemes to reduce the power consumption as with different node technologies. In the proposed work R2R DAC based SAR ADC is implemented but with 10-bit resolution and higher sampling rate (150 MS/s) and the main objective is to reduce power consumption of SAR ADC and improve ENOB and SNR of SAR ADC.

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

Table 1: Summary of the related work.

Parameters	Zhang Hao et al. [4]	Liu Haizhu and Maliang Liu [5]	Singh et al. [6]	Hequan Jiang et al. [7]	Xie Yi et al. [8]
Architecture	SAR	Pipelined-SAR	SAR	SAR	VCO-SAR
Technology (nm)	90	65	90	65	180
Resolution (bits)	10	12	8	10	10
Sampling Rate (MS/s)	120	200	250	160	5
Total Power (mW)	3.24	7.3	0.98	2	2.36
Active Area (mm^2)	-	0.21	-	0.023	0.126
SNDR (dB)	60.27	61.9	-	-	56.7
ENOB (bit)	9.72	10	-	8.9	9.13
FOM (J/conv-step)	32f	35.6f	-	25.4f	0.845p

3 SAR ADC KEY BUILDING BLOCKS

SAR-ADC features moderate circuit complexity, medium conversion speed and offer higher accuracy of conversion. SAR-ADC is widely accepted Nyquist rate data converter. The “Binary Search Algorithm” best describes the fundamental principal of SAR ADC functions with medium speed of conversion, moderate complexity of circuit and high accuracy of conversion. SAR-ADC is one amongst the accepted Nyquist rate data converters. The fundamental principles of SAR data converter can be best described by the “Binary search algorithm”. A SAR converter gives a proper balance between resolution, power consumption, conversion speed, size, and complexity of circuit. Successive Approximation Register architecture makes use of Binary search algorithm. The general block diagram in fig.1 illustrates various blocks of SAR-ADC that comprises of DAC block, comparator [9] block, sample and hold circuit block and SAR logic block. SAR logic block basically consist of shift register arrays along with decision register and decision logic. The circuit halves the sampled input signal (Vin) and the DAC output during the binary search (Vref.). Once the start of Conversion signal gets asserted the SAR ADC starts sampling the input signal and identifying the equivalent code for the analog sampled value. The Mega Speed Broadband (MSB) bit is set to high so that the DAC output remains at the midscale of its output. The comparator then checks for polarity of comparison for Vin and Vref. The pointer then sends the comparator's logical output to MSB. If Vin is greater than Vref (Vin> Vref), the register MSB is kept high (1), otherwise it is set to low (0).

The pointer, next, points to the bit next to MSB on the right side of MSB and is set to 1 (high). After the obtained DAC value gets settled to new value, the comparator again checks for polarity and previous steps get repeated. Once the SAR block is

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

done with obtaining digital value for the analog input signal it asserts End of Conversion signal. The entire architecture of the SAR ADC consist of four main fundamental blocks or modules namely DAC (Digital to Analog Converter), Comparator, Sample and Hold Circuit, Asynchronous SAR control logic.

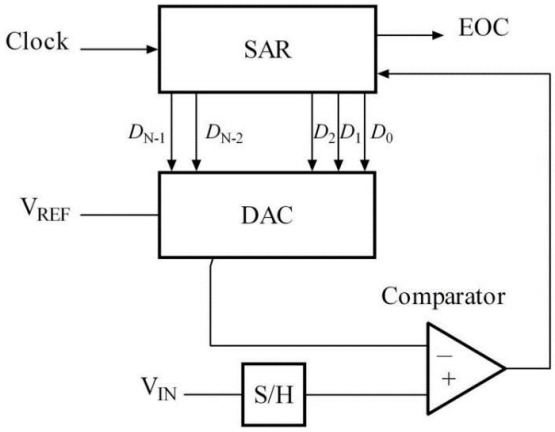

Figure 1: The detailed block diagram of SAR ADC architecture.

If the Sample and hold circuit provides the proper and necessary linearity and speed, the comparator referred input noise tends to become too small and data converters performance mainly depends on the DAC. To be precise INL and DNL of converter will be specified by DAC and the maximum speed of conversion is limited by settling time of DAC outputs. During the first conversion cycle the output of DAC has to settle to upper limit resolution of system so as to allow comparator to determine MSB precisely. If the time period of the clock is fully steady, then the conversion cycles that follow will be same as that of first one which implies that rate of conversion is limited by speed, the DAC posses.

3.1 Sample and Hold Circuit

Sample and hold (S/H) [10] circuit is a very crucial analog block used for many applications, including switched capacitor filters and Analog to Digital Converters (ADC). The sample and hold circuit's sole purpose is to sampling out an analog signal and store sampled result for later processing. Most of the ADCs make use of a sample-and-hold circuit at the front end which should be capable of attaining high precision, high speed and high linearity with very minimal power dissipation. The basic sample and hold circuit is depicted in fig.2. Amongst the various factors that affect the performance of basic sample and hold circuit are explained below.

When the clock (ϕ) to the NMOS is set to high, charge injection happens. When a clock is asserted to high, NMOS is activated, and input voltage is sampled using sampling capacitor (C_S). The charge gets accumulated under the gate oxide due to

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

inverted channel which can be computed using formula (1).

$$Q_{ch} = WLC_{ox}\left(V_{dd} - V_{in} - V_{tn}\right) \quad (1)$$

Next the transistor NMOS will thereafter be turned off when a clock signal (ϕ) becomes low. The charge that has built up beneath the gate oxide will get flushed out of the gate of NMOS to its drain and source, causing a voltage sample error. If suppose the entire charges get injected into the sampling-capacitor (C_S), then , voltage of the sampled- output is provided by equation (2).

$$V_{out} = V_{in}\left(1 + WLC_{ox}/C_S\right) - \left(WLC_{ox}/C_S\right)\left(V_{dd} - V_{tn}\right) \quad (2)$$

Thus, from the equations it is clear that the sampled output-voltage is being affected by the two factors, namely non-unity gain $\left(1+\left(WLcox\right)/C_S\right)$ and a constant offset voltage $\left(WLC_{ox}/C_S\right)\left(V_{dd} - V_{tn}\right)$.

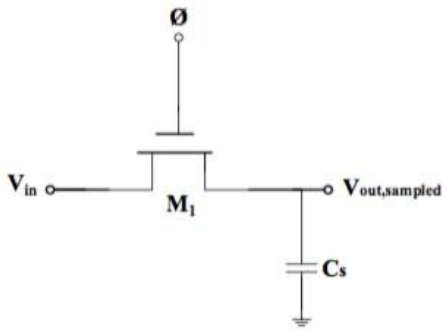

Figure 2: Basic sample and hold circuit

Clock feedthrough is defined as the pairing of transitions of clock and capacitor used for sampling by the CMOS transistor through its gate-source or gate-drain overlaplapping capacitances. When, the clock (ϕ) is high, an overlap-capacitance will be fed through gate-drain, gate- source, or both. While the transistor is off, a capacitive-divider will get created. This operations end impact is an offset-voltage, given in equation (3).

$$\Delta V_{offset} = \left(C_{OV}/\left(C_{OV} + C_S\right)\right)V_{dd} \quad (3)$$

where, C_{OV} is the overlap capacitance.

The topology of a sample-hold circuit with transmission gate(TG) helps in overcoming the effects of charge-injection and also clock-feed-through. This is accomplished by substituting a single NMOS transistor, in the fig.2 with the Transmission-Gate (TG) transistor as illustrated in the fig.3. If suppose, size of the P-MOS transistor in the transmission gate (TG) is the same as that of the NMOS

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

transistor, charge injection from both NMOS and PMOS is negated when a transmission gate is switched off. When the input-voltage(V_{in}) is very close to the supply-voltage(V_s), the PMOS transistor improves the ON conductance between the inputs and outputs of the TG. fig. 4 depicts the design of a TG-based Sample and Hold Circuit in cadence. Transistor aspect values for Sample and hold circuit is 2 for PMOS (W/L) and NMOS (W/L).

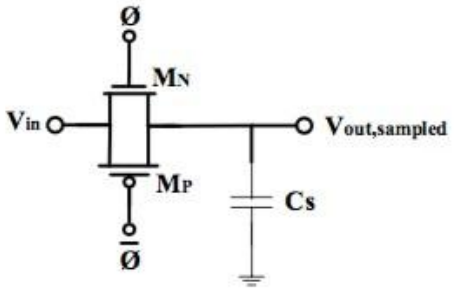

Figure 3: Sample and hold with transmission gate (TG)

The sample and hold using Transmission Gate (TG) consist of a parallely connected N-MOS and P-MOS. The gate-voltages(ϕ) applied to gates of PMOS and NMOS are complementary (Clk' and Clk) to each other. Transmission Gate is a bidirectional switch that connects the input Vin to the output Vout controlled by the clock signal. The PMOS gate is connected to Clk', whereas the NMOS gate is connected to Clk. Both transistors are ‘on’ when the control signal Clk is high, resulting in a low resistance route between Vin and Vout. When Clk is low, however, both transistors are switched off, resulting in a high-impedance route between Vin and Vout. The capacitor here stores the sampled output (500 fF). fig. 5 illustrates the transient analysis of the Sample and Hold circuit.

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

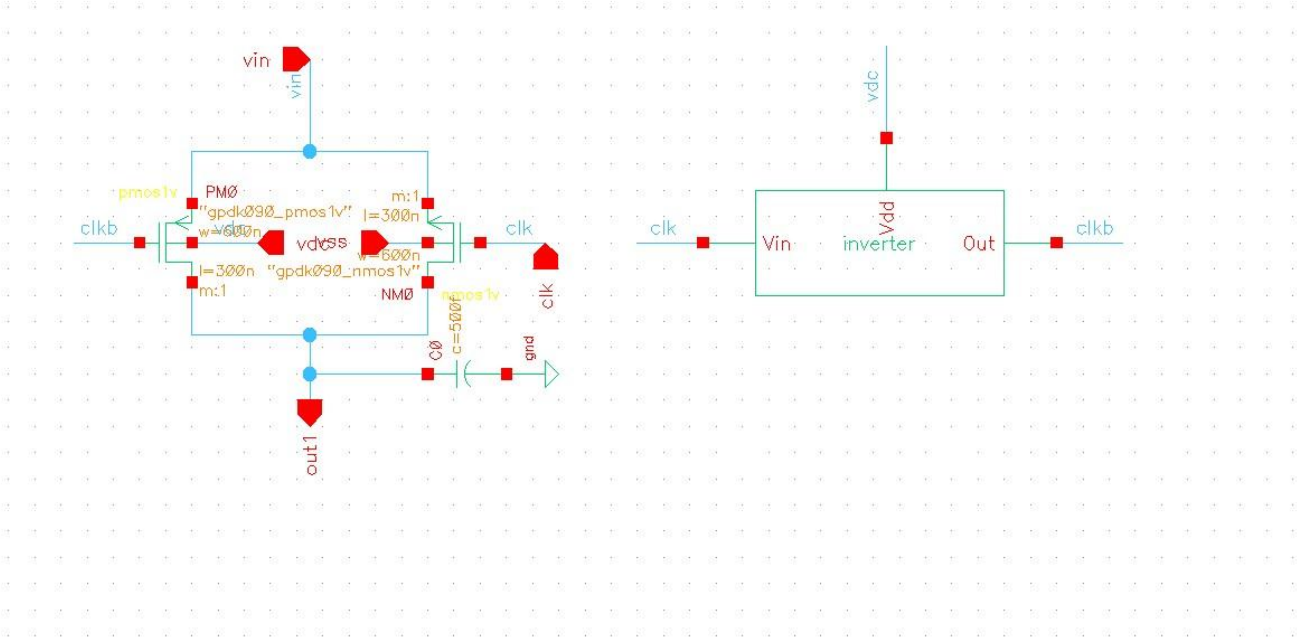

Figure 4: Cadence implementation of TG based sample and hold circuit

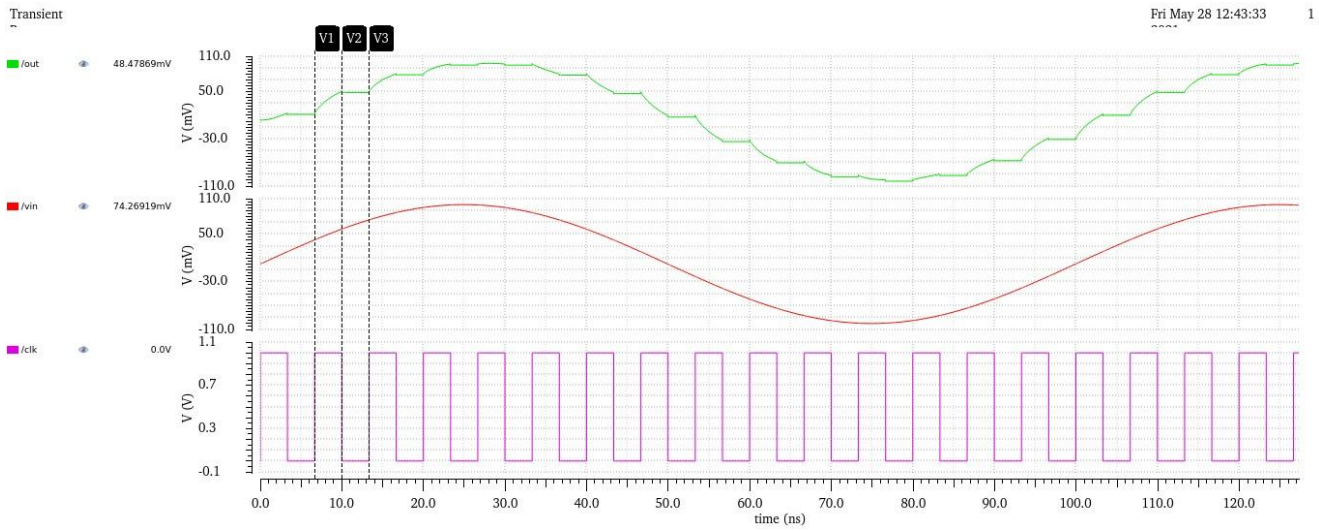

Figure 5: Transient analysis of sample and hold circuit

3.2 COMPARATOR

Comparator plays a vital key role in many of the Analog to Digital Converters. It is an essential basic building block, for the applications where, the digital-information needs to be retrieved from analog-signals, like ADC, memory bit-line detectors and I/O data-receivers . The Comparator [11] used in ADC should have sufficiently high gain so that even a small change in input will result in firmly switching of the output level. In this paper of SAR-ADC, a high gain Operational amplifier (op-amp) [12] is

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

being used as a comparator so that output switching of a comparator will remain firm even though there will be a small change in comparator input. The general block diagram of Operational amplifier is shown in fig.6. The Operational amplifier that we are intended to design will have high PSRR and high gain. The operational amplifier designed will have two stages of which, the first stage of op-amp attenuates the power and noise and second stage rejects the noise which might be present at its common inputs. With this architecture of op-amp ,it is, possible to attain high PSRR and high gain. As shown in the fig. 6, first stage consists of transistors M1 till M5 and stage two consists of transistors M6 and M7. The circuit diagram also represents how each transistor in the circuit are associated with the specification of Op-Amp. For example, the bias current I5 depends on the slew rate and the phase margin can be compensated with compensation capacitor (Cc).

The same design operational amplifier is being used as comparator [13] in this paper as shown below in fig.7. The output (Vin) of the sample and hold circuit will be connected to positive terminal of Op-amp and DAC output (Vref) is connected to negative terminal of comparator. Suppose if Vin exceeds Vref the output of the comparator will be set high and if Vin is less than Vref comparator output will be set low. The Op-Amp implementation in cadence is as shown in fig.6. The AC analysis of Op-Amp is as shown in fig.8. The test bench implementation of Op-Amp as comparator is shown in fig.7. The comparator output is shown in figure 9. The aspect ratios of transistors and outputs for operational amplifier is given in table 2.

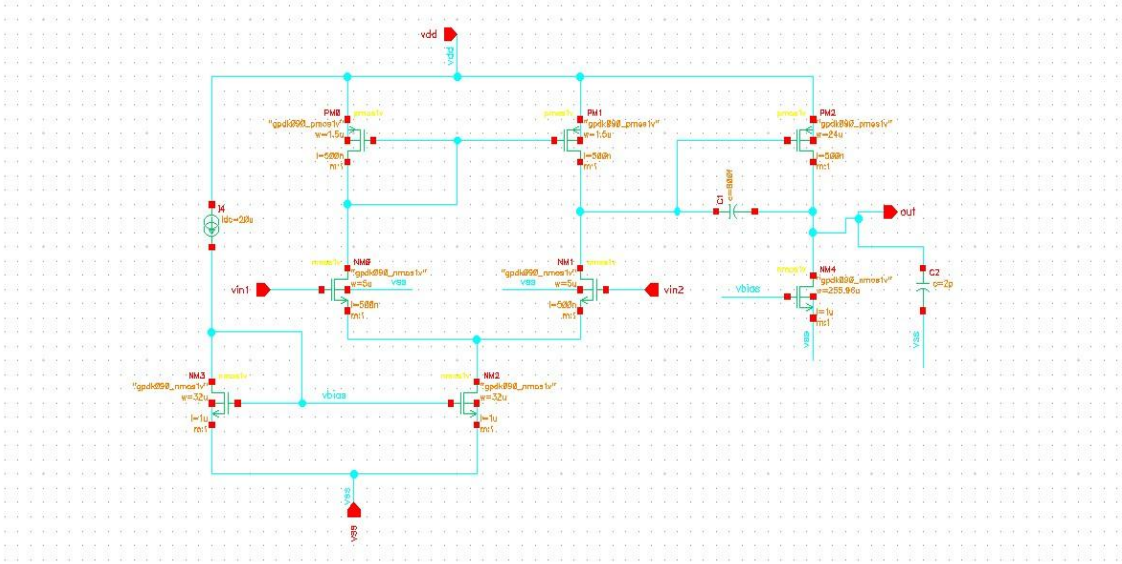

Figure 6: Schematic of operational amplifier in cadence

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

Table-2

Parameter	Value
Technology	90 nm
VDD	1 V
$(W/L)_{1,2}$	10
$(W/L)_{3,4}$	3
$(W/L)_{5,8}$	32
$(W/L)_6$	48
$(W/L)_7$	256
Load Capacitor (C_L)	2 pF
C_C	800 fF
I_{REF}	20 uA
Gain	66.97 dB
Phase margin	60.03
Gain Bandwidth	29.66 MHz

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

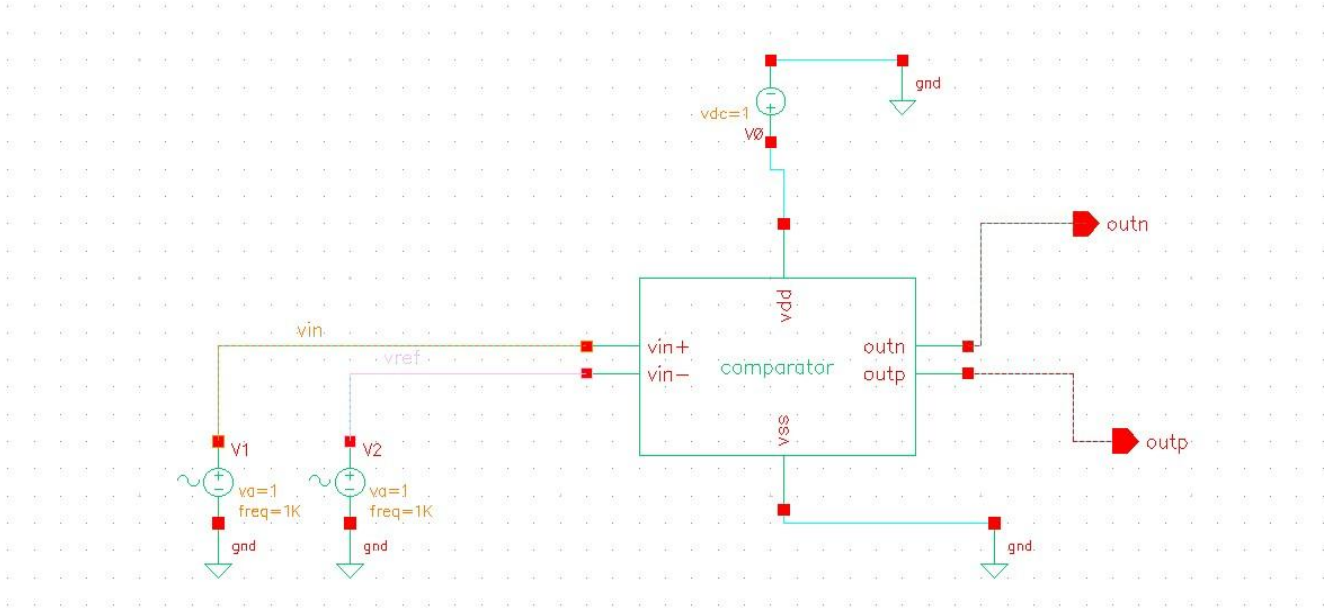

Figure 7: Comparator test bench

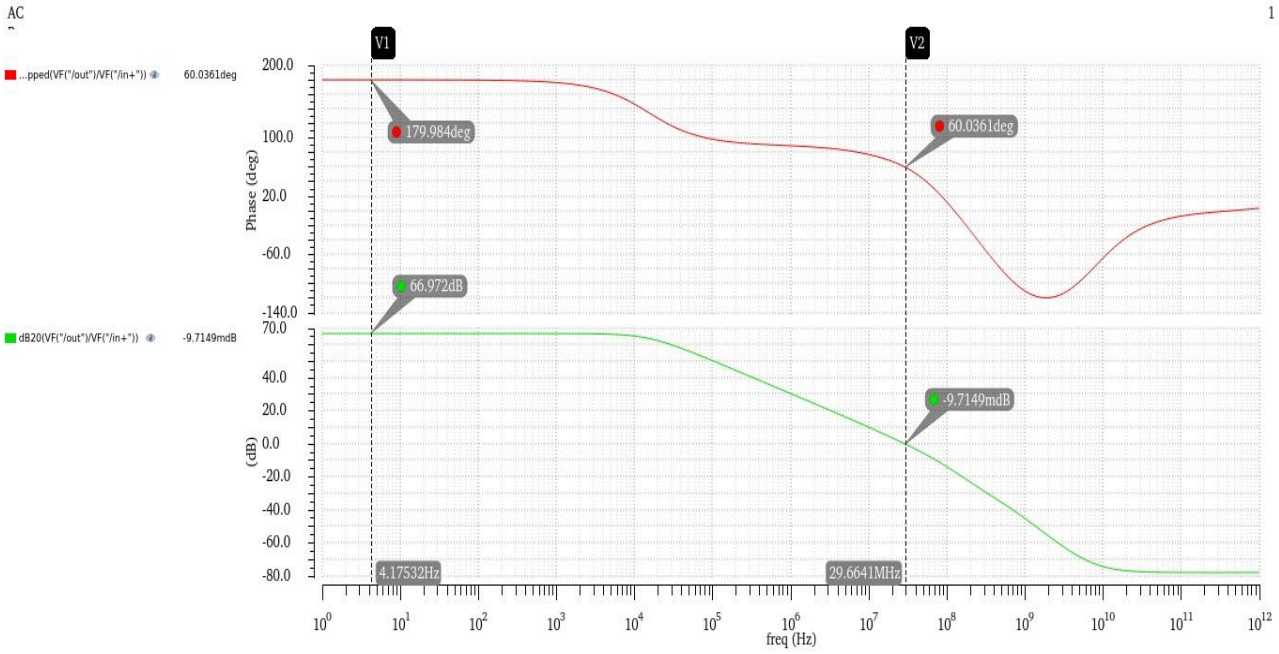

Figure 8: AC analysis

As shown in fig. 9, when Vin+ exceeds Vin- output of comparator will be set to high and when Vin+ is less than Vin- the comparator output is set low.

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

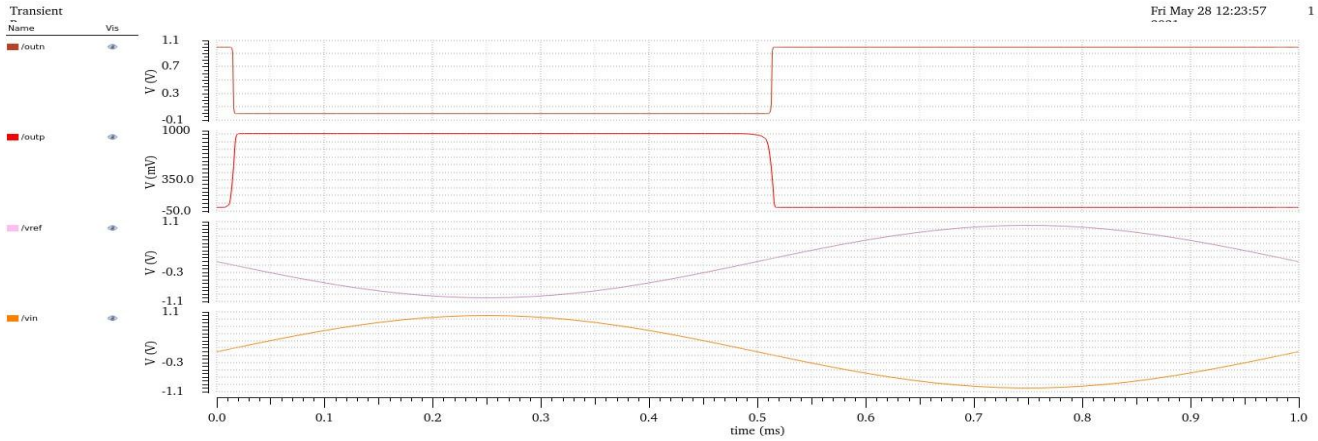

Figure 9: Output of comparator

3.3 R2R Structure Digital to Analog Converter

The R2R Resistive DAC[14] is a ‘‘binary weighted‘‘ Digital to Analog Converter that uses repeated cascade structure of resistors as shown in fig. 10. The main advantage of R2R resistive DAC is that it uses resistors of only two-values namely R and 2R, and also uses minimal number of components. This helps in enhancing the precision due to ease of getting equally valued matched resistors. The main drawback of this R2R resistive DAC is that as the resolution of DAC increases the number of switches and resistors also increases and hence there will be relatively more time delay between MSB and LSB and therefore the value of resistors must have very high linearity[15].

A 2:1 mux is used as switch in R-2R resistive DAC as shown in figure 11. In figure 13 R-2R ladder structure is shown whose output is connected to operational amplifier in voltage follower configuration. The simulation results is shown in figure 12.

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

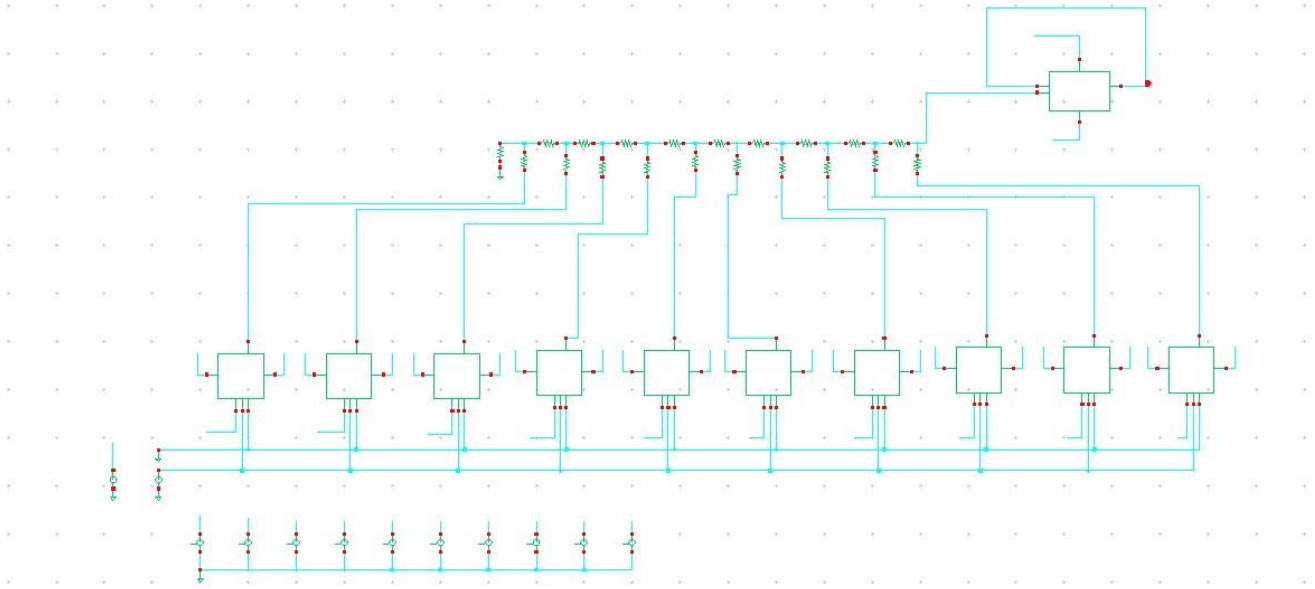

Figure 10: Schematic of R-2R resistive DAC

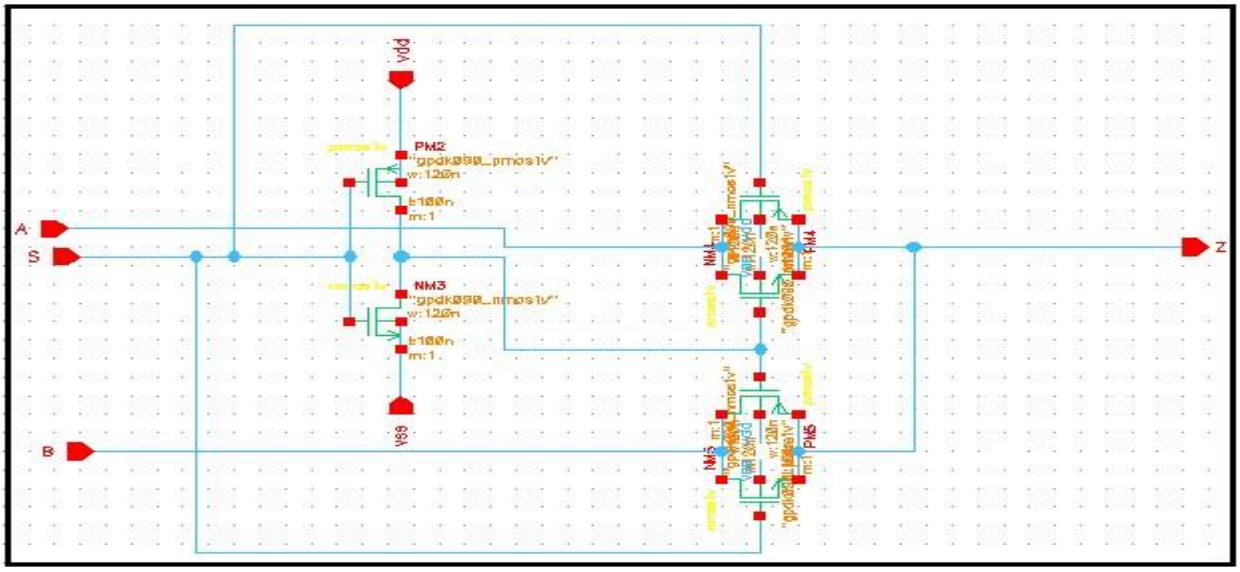

Figure 11: Schematic of 2:1 mux

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

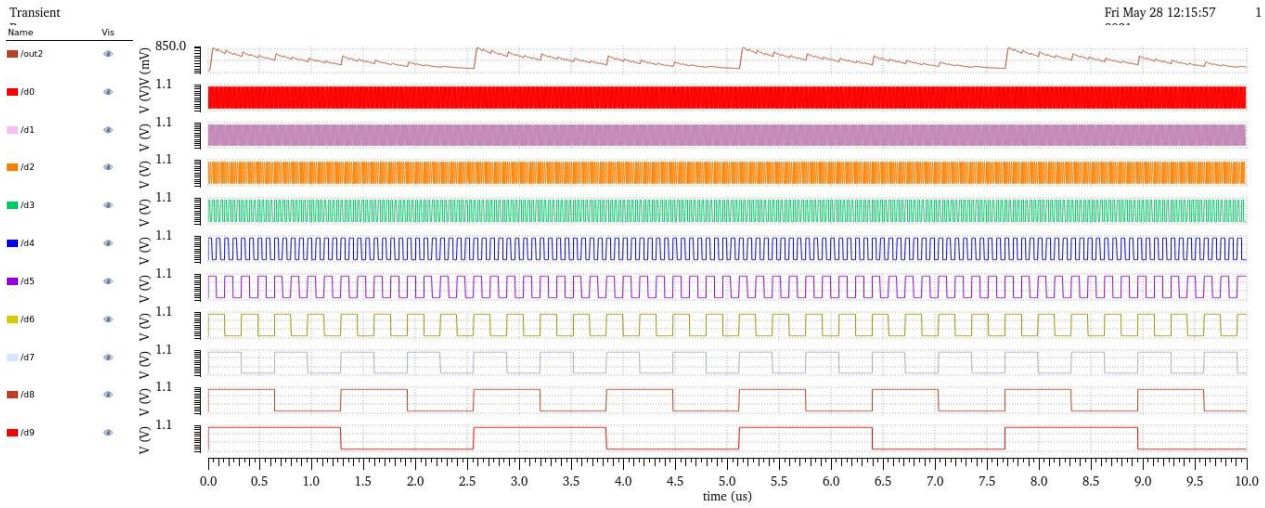

Figure 12: Output of R-2R DAC

3.4 The SAR Logic

The successive approximation register (SAR) is a digital-controller circuit that implements the "binary search algorithm". The comparator output will be used to determine the output, which will be the digital counterpart of the analog input value. As a result, it has a significant impact on the overall performance of the ADC, which in turn has an impact on the entire system. The DAC, comparator and SAR logic are the major power-consumption in a SAR-ADC[16],[17] converter. The D flip flop[18] clock-gated SAR logic controller is being made use of in order to minimise overall clock system's power-consumption. fig 13 depicts the D Flip-flop block diagram.

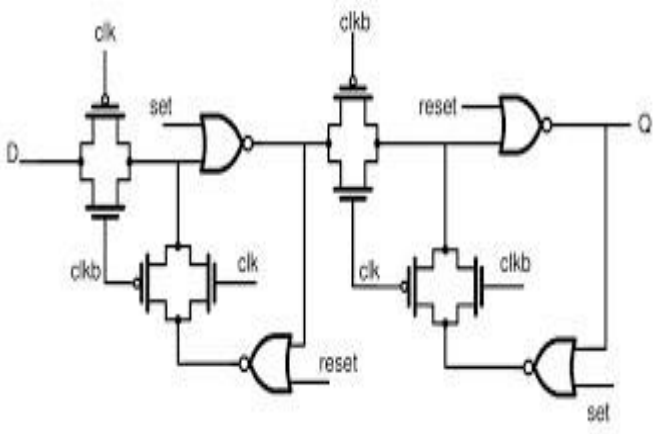

Figure 13: Block diagram of D flip-flop

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

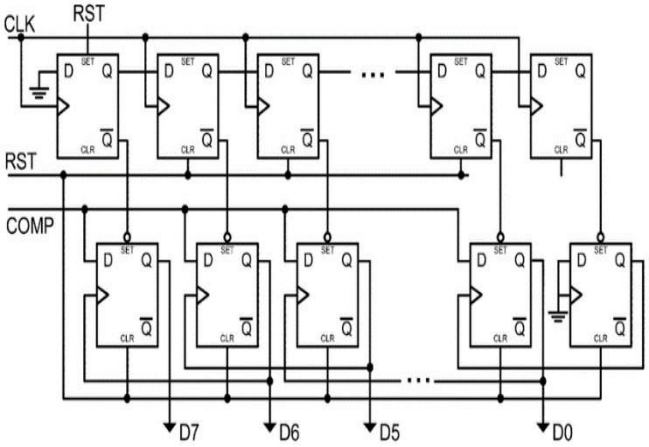

Figure 14: Block diagram of SAR logic

The schematic of SAR logic block using D flip-flops [19] is shown in fig.14. The SAR logic block consists of two arrays of shift register. The topmost array acts as sequencer to the bottom array of shift register .The bottom array does the actual job of binary search and stores the digital equivalent value of analog signal as per the comparator output. The topmost array is synchronous while the bottom array is made asynchronous to reduce power consumption of SAR logic. The cadence implementation of D Flip-flop is depicted in fig.15. The output of D Flip-flop is captured in fig.16. The D Flip flop output is set low when reset is set high [20] and when the set signal is asserted the output of D Flip-flop remains high. In other cases the output is same as input with delay of one clock cycle. The SAR logic block consists of arrays of D Flip-flops. The schematic of SAR block is shown in fig.17.

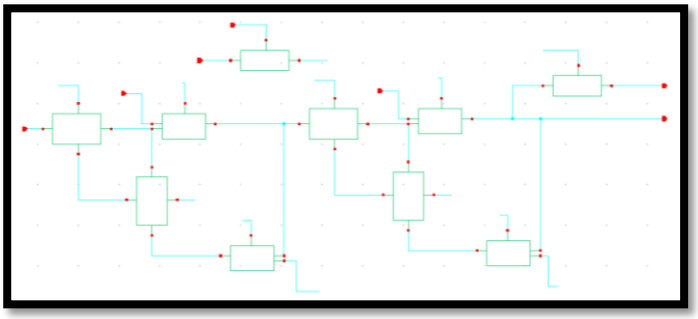

Fig 15. Cadence implementation of D Flip-Flop shown in fig.13

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

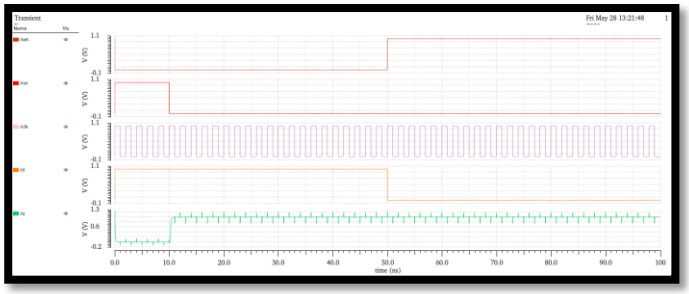

Fig 16. Simulation result of D Flip-flop

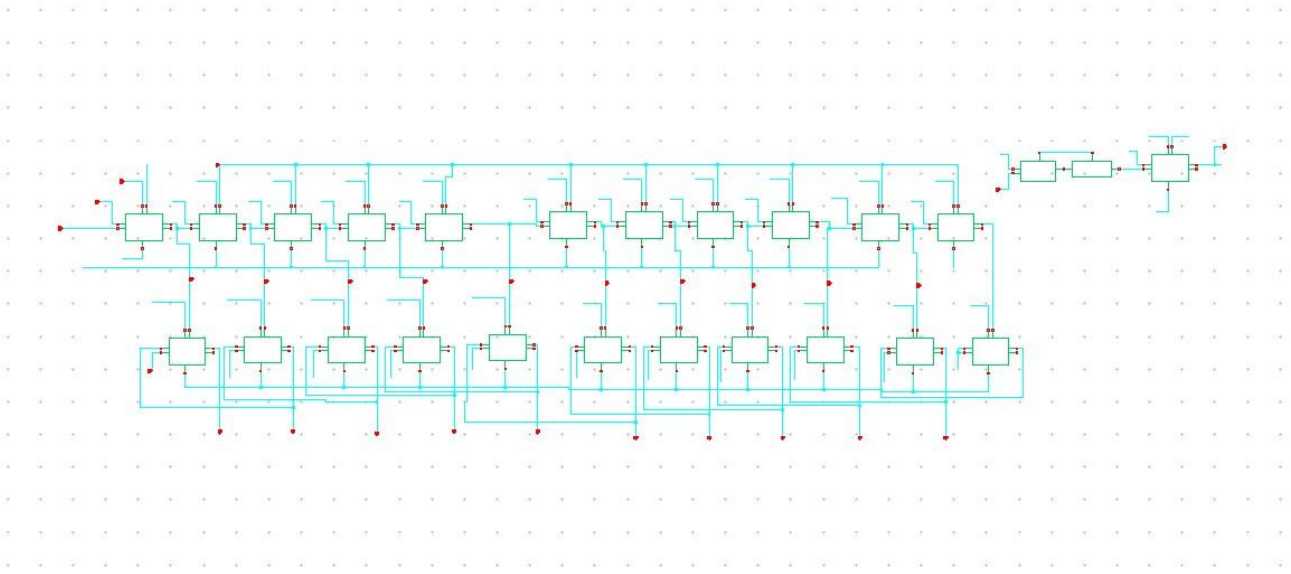

Figure 17: Cadence implementation of SAR structure shown in figure 14

3.5 Integration of 10 Bit SAR ADC

The fig. 18 depicts the complete SAR ADC which consist of a 10-bit DAC stage block, which includes a transmission gate-based sample and hold circuit, 10-bit DAC, Comparator and SAR logic block. The analog input is supplied to sample-hold circuit and sampled output along with analog output from DAC is given to comparator. The output of [21] comparator is fed to SAR block to get digital output. The digital output is fed back to DAC for generating analog [22] equivalent. The schematic of complete SAR ADC is as shown in fig.18 and the complete 10-bit simulation is dipicted in fig.19.

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

4 RESULTS AND DISCUSSION

The aspect ratios of transistors used in the high gain operational amplifier is shown in table 2. From simulation results, shown in fig. 8, the gain of the Operational amplifier is 66.97 dB and phase margin is 60.03 degree. The gain bandwidth is found to be 29.66 MHz. The power consumption of Operational amplifier is found to be 185 µW. The design of SAR ADC using Resistive R2R DAC is implemented for 10 bits in 90nm CMOS technology using cadence virtuoso schematic editor tool. The results are shown in table 3. As shown in table 3, it can be observed that, this work consumes less power compared to proposed architectures. The power consumption of SAR ADC in this work is 265.8µW. The ENOB is 9.39-bits and this work is having SNDR of 58.2dB. The INL and DNL of DAC output is 0.38 LSB. The SAR-ADC is implemented in 90nm CMOS process technology. Thus, from observations, one can conclusively state that the medical implants deployed inside a human body would last longer. Life cycle testing would however be required to find out as to how much longer the implants actually last.

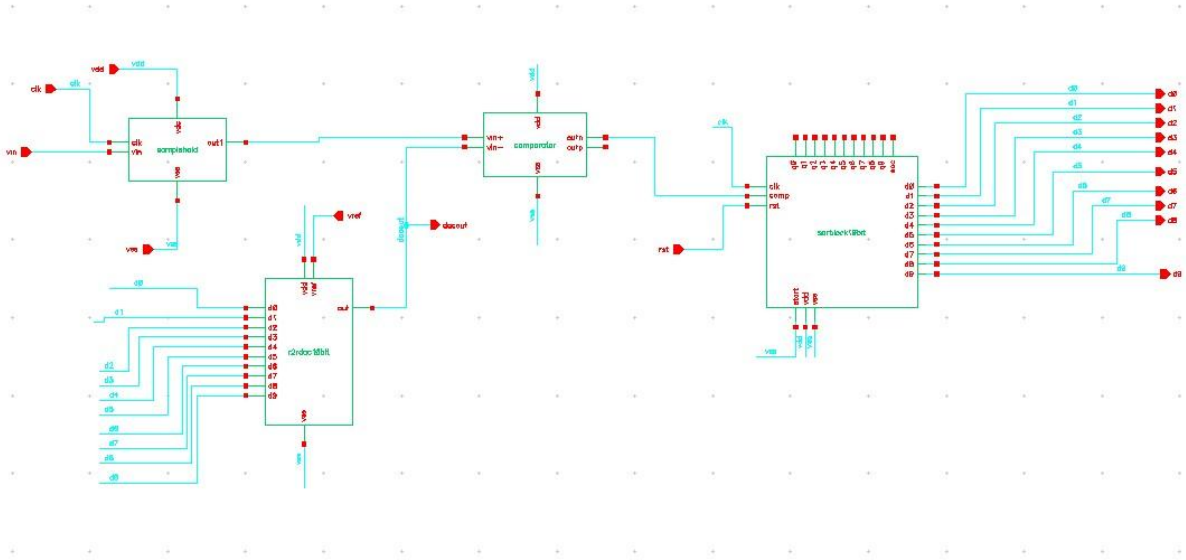

Figure 18: Schematic of cadence implementation of SAR ADC SAR ADC

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

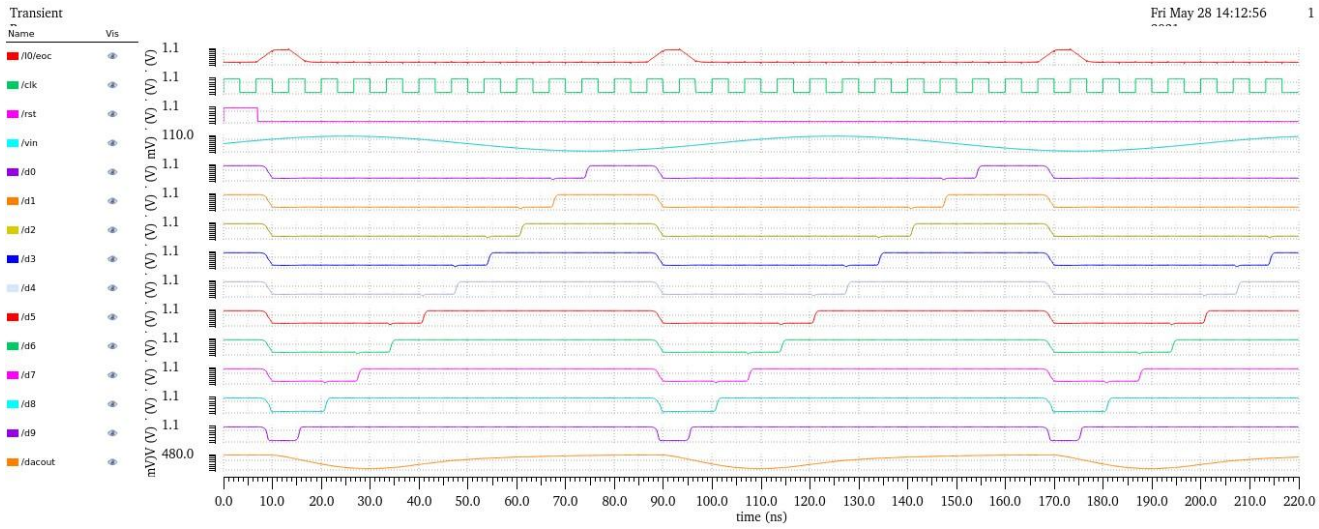

Figure 19: Simulation result of SAR ADC

5 CONCLUSION

In this paper, a resistive R2R DAC of 10-bit resolution SAR-ADC has been designed and implemented in 90nm CMOS process technology. The high gain Operational amplifier is used as comparator for deciding polarity of DAC and sample and hold output after comparison. A unique enhanced–linearity type 10-bit Asynchronous SAR ADC is suggested, featuring high gain comparator. R-2R resistive DAC is proposed with multiplexer-based switching. An improved SAR logic with Transmission-Gate (TG) based D Flip-flop, is also proposed to achieve further area reduction. The design of D flip-flop utilizes less area and less power. The suggested ADC is simulated using a 90nm CMOS technology with a 1V supply, and the results show that it performs better than earlier approaches. Finally, with ENOB of 9.39 bits and Differential and Integral nonlinearity of 0.38 LSB, the ADC has achieved, sampling rate of 150 MS/s. The consumption of power of SAR ADC is 265.8 µW which is 12 times less in comparison to base paper ADC power consumption which is 3.24mW. The suggested ADC is suitable for high-speed real-time applications based on these findings. Possible future work includes improved accuracy with the proposed structure of DAC, techniques to improve the power consumption and ENOB such as turning off the comparator during the sampling phase

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

Table 3: Comparison of results.

Parameters	Zhang Hao et al. [4]	Liu Haizhu and Maliang Liu [5]	Singh et al. [6]	Hequan Jiang et al. [7]	Xie Yi et al. [8]	Proposed method
Architecture	SAR	Pipelined-SAR	SAR	SAR	VCO-SAR	SAR
Technology (nm)	90	65	90	65	180	90
Resolution (bits)	10	12	8	10	10	10
Sampling Rate (MS/s)	120	200	250	160	5	150
Total Power (W)	3.24m	7.3m	0.98m	2m	2.36m	265.8u
Active Area (mm^2)	-	0.21	-	0.023	0.126	-
SNDR (dB)	60.27	61.9	-	-	56.7	58.2
ENOB (bit)	9.72	10	-	8.9	9.13	9.39
FOM (J/conv-step)	32f	35.6f	-	25.4f	0.845p	-
INL	-	-	0.35	-0.97 / +0.93	-	0.38
DNL	-	-	0.38	-0.75 / +0.47	-	0.38

REFERENCES

[1] Q. Fan and J. Chen, "A 500-MS/s 13-Bit SAR-Assisted Time-Interleaved Digital-Slope ADC," 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 2019, pp. 1-5, doi: 10.1109/ISCAS.2019.8702383.

[2] K. Kuo, "A 10-bit 250 MS/s Binary Search and Two channel SAR ADC by a two-bit per Conversion with Error Tolerance Ability," 2019 International SoC Design Conference (ISOCC), Jeju, Korea (South), 2019, pp. 1-2, doi: 10.1109/ISOCC47750.2019.9027763.

[3] H. Liu, M. Liu and Z. Zhu, "A 12-bit 200MS/s Pipelined-SAR ADC in 65-nm CMOS with 61.9 dB SNDR," 2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Xi'an, China, 2019, pp. 1-2, doi: 10.1109/EDSSC.2019.8754022.

[4] Zhang, Hao, Xinghua Wang, Lei Zhang, and Zhijing Zhang. "A 10-bit 120-MS/s SAR ADC in 90nm CMOS with redundancy compensation." In 2018 IEEE MTT-S International Wireless Symposium (IWS), pp. 1-3. IEEE, 2018.

[5] Liu, Haizhu, Maliang Liu, and Zhangming Zhu. "A 12-bit 200MS/s Pipelined-SAR ADC in 65-nm CMOS with 61.9 dB SNDR." In 2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), pp. 1-2. IEEE, 2019.

[6] Gaurav Kumar Sharma, Singh, Vijay Pratap, and Aasheesh Shukla. "Power efficient SAR ADC designed in 90 nm CMOS technology." In 2017 2nd International Conference on Telecommunication and Networks (TEL-NET), pp. 1-5. IEEE, 2017.

[7] Xu, Daiguo, Lei Qiu, Xiaoquan Yu, Hequan Jiang, Jianan Wang, Can Zhu, Shiliu Xu and Zhengping Zhang. "A Linearity-Enhanced 10-Bit 160-MS/s SAR ADC With Low-Noise Comparator Technique." IEEE Transactions on Very Large Scale Integration (VLSI) Systems (2019).

[8] Xie, Yi, et al. "A 10-Bit 5 MS/s VCO-SAR ADC in 0.18-um CMOS." IEEE Transactions on Circuits and Systems II: Express Briefs 66.1: pp. 26-30. IEEE,2018.

[9] V. Mallapur ,H.P. Le, J. Singh, A. Stojcevski and L. Hiremath "Ultra-low-power variable-resolution successive approximation ADC for biomedical application", Electronics Letters 26th May 2005 Vol. 41 No. 11.

Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol:54 Issue:11:2021
DOI 10.17605/OSF.IO/M5N68

[10] Reza Lotfi and Samaneh Babayan-Mashhadi ," Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator", IEEE Transactions on Very Large Scale Integration (VLSI) Systems Vol. 22, Issue: 2, Feb. 2014.

[11] Rajesh Mehra and Priyanka Sharma , "True Single Phase Clocking Based Flip-Flop Design Using Different Foundries", International Journal of Advances in Engineering & Technology, May, 2014.

[12] Mr. Ganesha H.S, Dr. Rekha Bhandarkar and Ms. Vijayalatha Devadiga, " A 8-Bit Hybrid Architecture Current-Steering DAC", International Research Journal of Engineering and Technology (IRJET), Volume: 02 Issue: 04 | July-2015.

[13] G.M.Lee and C.Hong, "A 65-fJ/conversion-step 0.9-V 200-kS/s rail-to-rail 8-bit successive approximation ADC", IEEEJ. Solid-State Circuits 42(10) (2007) 2161–2168.

[14] Hwang-Cherng Chow and Yi-Hung Chen, "1V 10-bit Successive Approximation ADC for Low Power Biomedical Applications", Published in: Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference.

[15] Santanu Sarkar and Swapna Banerjee, "An 8-bit 1.8 V 500 MSPS CMOS Segmented Current Steering DAC", IEEE Computer Society Annual Symposium on VLSI, 2009.

[16] C.G.Cheng, S.Y.Lee, S.C.Lee, C.P.Wang, "A 1-V 8-Bit 0.95 mW successive approximation ADC for biosignal acquisition systems", in: Proceedings of the IEEE International Symposium on Circuits and Systems, vol.42,no.10, May.2009, pp. 649–652.

[17] Dai Zhang, Atila Alvandpour and Ameya Bhide, "A 53-nW 1-kS/s SAR ADC in 0.13-µm CMOS for Medical Implant Devices", Published in: ESSCIRC (ESSCIRC), and IEEE 2011.

[18] S.Sivasathya and T.Manikandan, "Design of Double Tail Comparator for High Speed ADC ", International Journal of Innovative Research in Computer and Communication Engineering, Vol.2, Special Issue 1, March 2014.

[19] Mrs. Jasbir Kaur and Saurabh Kansal, " Study of Various ADCs and Compare Their Performance and Parameters", International Journal of Advanced Engineering Research and Technology (IJAERT), Volume 3 Issue 3, March 2015,

[20] Er. Swarnjeet Singh, Hardeep Kaur and Sukhdeep Kaur, " Design and Analysis of D Flip Flop Using Different Technologies", IJIRCCE, Vol. 3, Issue 7, July 2015.

[21] Tasnim B. Nazzal and Soliman A. Mahmoud, " Sample and Hold Circuits for Low-Frequency Signals in Analog-to-Digital Converter", 2015 International Conference on Information and Communication Technology Research (ICTRC2015).

[22] S. Oh et al., "A 80dB DR 6MHz Bandwidth Pipelined Noise-Shaping SAR ADC with 1–2 MASH structure," 2020 IEEE Custom Integrated Circuits Conference (CICC), Boston, MA, USA, 2020, pp. 1-4, doi: 10.1109/CICC48029.2020.9075929.